Biyani's Group of Girls' Colleges

Model Paper – II

Examination-2016

BCA III

Advanced Computer Architecture

Time: 3 Hrs. MM:50

I) The Question paper contains 40 multiple choice questions with four choices and student will have to pick the correct one (each carrying ½ mark).

1. The number of edges incident on a node is called:
   (a) Node degree (b) Node diameter
   (c) Network degree (d) Network diameter

2. Harold stone (1971) introduced special permutation function that was:
   (a) Multicast (b) Perfect Shuffle
   (c) Broadcast (d) Routing

3. Multi-processor, vector-supercomputer, and multi computer were appeared in:
   (a) 1st generation (b) 2nd generation
   (c) 3rd generation (d) 4th generation

4. Which is not valid architecture of a vector super computer?
   (a) Register to register (b) Memory to memory
   (c) Both a and b are invalid (d) None of the above

5. One nibble is equivalent to:
   (a) 8 bits (b) 4 bytes
   (c) 8 bytes (d) 4 bits

6. Instruction to be executed resides:
   (a) Program counter (b) Accumulator
   (c) MBR (d) Instruction Register

7. Two or more CPU's present in a computer system which share some or all of the memory called:
   (a) Paralled (b) Multipgramming
   (c) Multi tasking (d) Random File processing

8. Barrel shiffer is a:
   (a) Static connection network (b) Dynamic connection network
   (c) Storage device (d) Switching device

9. Which is the valid vector access memory scheme?

(a) C-Access memory organization
(b) Asynchronous
(c) Synchronous memory organization
(d) D-Access memory organization

10. The full form of PRAM is:
(a) Parallel Random Access Machine
(b) Parallel Remote Access Machine
(c) Powerful Random Access Memory
(d) Partial Random Access Memory

11. .....is a process of moving blocks of information between the levels of memory hierarchy:
(a) Memory swapping
(b) Memory allocation
(c) Memory interleaving
(d) Memory scheduling

12. In binary tree network the bisection width would be:
(a) 1
(b) 2
(c) N/2
(d) $\{N/2\}^2$

13. Pipelining is:
(a) Programming technique
(b) Decomposing of sequential process into sub operations
(c) Hardware module
(d) None

14. In general vector processing is faster and.....scalar processing:
(a) Less efficient than
(b) Equally efficient to
(c) More efficient than
(d) None of the above

15. The memory connected to the common system bus is.....by all processors.
(a) Shared
(b) Partitioned
(c) Distributed
(d) None of the above

16. A typical system bus consists of approximately.....signals lines
(a) 100
(b) 2
(c) 3
(d) None of the above

17. Which is not a valid data routing function?
(a) Perfect shuffle and exchange
(b) Permutation
(c) Multicast
(d) Broadband

18. MAL stands for:
(a) Minimal Average Latency
(b) Minimum Allocation Latency
(c) Maximum Allocation Latency
(d) Maximum Average Latency

19. .....computing is achieved through the use of an array of processing elements synchronized by the same controller;
(a) MIMD
(b) SIMD
(c) Both a and b
(d) None of the above

20. The speed of microcomputer measure in:
(a) MIPS
(b) Picoseconds
(c) Megahertz
(d) Milihertz

21. The pipeline used for floating point operations is called:

(a) Arithmetic pipeline (b) Instruction pipeline
(c) Both (a) and (b) (d) None of the above

22. A.....can be be visualized as a collection of processing segments through which binary information flows:
(a) Memory (b) I/O devices
(c) Processor (d) Pipeline

23. A memory deices in which a bit is stored as a charge across the stray capacitance:
(a) SRAM (b) EPROM
(c) DRAM (d) Bubble Memory

24. The size of virtual memory depends on:
(a) The size of data bus (b) The size of the main memory
(c) The size of the address bus (d) None

25. Loosely coupled system are more efficient when the interaction between task is:
(a) Maximum (b) Minimum
(c) Can not say (d) None of the above

26. The memory used in a computer system is based on the following principle:
(a) Principle of parallel computing (b) Principle of concurrent occur
(c) Principle of locality (d) None

27. Processors that use multiphase clocks with a muck increase clock rate ranging from 100 to 500 MHz are:
(a) VLIW (b) RISC
(c) Memory interleaving (d) Super view

28. The time in cycles required between the issuing of two adjacent instruction is:
(a) Instruction issue rate (b) Instruction pipeline cycle
(c) Instruction operations latency (d) Instruction issue latency

29. The main objective of scheduling evnets in a pipeline is:
(a) to obtain shortest latency between initiations without causing cohesion
(b) to obtain highest latency between initiations without causing collisions
(c) To obtain shortest latency between initiations without causing collisions
(d) All of the above

30. Memory interleaving is:
(a) Modular memory (b) Virtual memory
(c) Shared memory (d) Cache memory

31. VLIW stands for:
(a) Very Long Instruction Word (b) Very Long Instruction Word
(c) Very Large Information Word (d) None of the above

32. Flynn's classified parallel computers into.....categories.
(a) 2 (b) 3
(c) 4 (d) 8

33. .....Networking are controlled by a global clock.
(a) Asynchronous (b) Synchronous
(c) Both (a) and (b) (d) None of the above

34. Bootstrap is:
(a) A memory device (b) a device to support the computer
(c) A startup correction technique (d) an error correction technique

35. Multi-programming is:
(a) A technique to perform more than one task in memory
(b) Capability to keep more than one program
(c) A technique to perform paralel processing
(d) None of the above

36. The size of program is determined by:
(a) Clock rate (b) Clock count
(c) Instruction execution (d) Instruction count

37. The portion of the operating system kernel which handles the allocation and deallocation of main memory to executing processes is called:
(a) Memory Swapper (b) Memory Manager
(c) Process Swapper (d) Process Manager

38. For inter PE data exchange network that is used be:
(a) Static (b) Dynamic
(c) Either a or b (d) None of the above

39. Three dimensions of locality property are:
(a) Temporal, parallel and sequential (b) Temporal, spatial and sequential
(c) Spatial, parallel and sequential (d) None of the above

40. .....consist of an address transfer followed by a block of I or more data to 1 or more contiguous addresses:
(a) Address only transfer (b) Packet data transfer
(c) Evaluation cycle (d) All of the above

II) Attempt any four questions out of the six. All questions carry 7½ marks each.

Q1. Explain Omega Network and Crossbar Network in detail.

Q2. Describe :
(i) Generations of electronic computers. (ii) Elements of modern computer

Q3. Explain all the factors on which the performance of interconnected network depends. Discuss the following dynamic connection networks.
(a) Digital buses
(b) Omega network

Q4. What is the difference between physical cache and virtual cache? Describe various block placement schemes of cache memory.

Q5. What do you understand with pipelining processor? Describe the arithmetic pipeline with the help of example.

Q6. (a) Discuss the terms data transfer bus (DTB) bus arbitration and control and Financial modules related to backplane bus.
(b) What do you mean by Backplane Bus system?